EU funded research project launched to investigate on reliable terascale memory systems

Barcelona, February 22nd, 2010. The European Commission has launched a joint FP7 Future Emerging Technology research project TRAMS aiming to investigate the impact of increasing variability and decreasing reliability of the components in future terascale memory systems and to create new design paradigms which can secure their reliable operation in future multicore processors and system on a chip applications. The TRAMS (Terascale Reliable Adaptive Memory Systems) project consortium includes Intel Corporation Iberia, the nanoelectronics research center imec, the University of Glasgow (UOG) and the Universitat Politècnica de Catalunya (UPC).

It is expected that as a result of continuing transistor miniaturization and performance improvement, described by the famous Moore's law, in the next decade a single chip will be able to perform many billions of operations per second and will provide many billions of bytes per second off-chip bandwidth. These terascale computing capabilities will transform not only the throughput of large data centers and computing facilities but also the power, the performance and the functionality of personal computers, communication devices, computer games and other consumer electronics products. However, the individual nanoscale transistors in the future terascale chips will be much more susceptible to manufacturing faults, will have unprecedented variability and will be more unreliable. The TRAMS project will be a bridge for delivering of reliable, energy efficient and cost effective computing in the era of nanoscale challenges and teraflop opportunities.

The project targets transistors, circuits and systems near the end of the International Roadmap for Semiconductors (ITRS) and beyond. A starting point will be the Late CMOS technologies after the 16 nm technology generation including novel multigate device architectures and novel channel and gate stack materials expecting to reach important scaling challenges below 10 nm dimensions. Beyond-CMOS emerging technologies such as nanowire transistors, quantum devices, carbon nanotubes, graphene, or molecular electronics are expected to scale below 5 nm. Both the Late CMOS and the Beyond CMOS technologies hold the promise of a significant increase in device integration density complemented by an increase in system performance and functionality. However, a dramatic reduction in single device quality is also expected, complemented by an increase in variability, severe reduction of the signal to noise ratio, and severe reliability problems. Therefore, alternative circuit and system solutions need to be investigated to deliver reliable systems out of variable and unreliable components and keep harvesting the benefits fueled by technology scaling. In this project we focus on the memory system of terascale processors.

Memory cells and, in general, system architectures for nanotechnologies (both late CMOS and emerging devices) need to address the variability and reliability problem. In order to build reliable nanosystems, the TRAMS project will apply a specific variability and reliability-aware analysis and design flow as well as a hierarchical tolerance design. The project will investigate novel solutions at circuit and architecture levels, which will be able to provide reliable memory systems out of unreliable nanodevices at a reasonable cost and design effort.

The Universitat Politècnica de Catalunya (UPC), BarcelonaTech, the Spanish technical university located in Barcelona is the project coordinator. The UPC is one of the main technical universities in Spain. It is specialized in the areas of engineering, science and architecture. It has around 30,000 undergraduate students and 4,000 graduate students (Master and Doctorate). The UPC participation in the TRAMS project is through the research groups "High Performance Integrated Circuits and Systems Design" (HIPICS) and "Architecture and Compilers" (ARCO) in the Electronics Engineering and Computer Architecture Departments respectively.

The University of Glasgow (UOG), The University of Glasgow is one of the top 20 research led universities in the UK from the Russell Group and one of the top 100 universities worldwide. It was established in 1451 and has 15000 undergraduate and 4900 postgraduate students. The Device Modeling Group from the Department of Electronics and Electrical Engineering led by Professor Asen Asenov represents the University in the TRAMS consortium.

Imec performs world-leading research in nanoelectronics. Imec leverages its scientific knowledge with the innovative power of its global partnerships in ICT, healthcare and energy. Imec delivers industry-relevant technology solutions. In a unique high-tech environment, its international top talent is committed to providing the building blocks for a better life in a sustainable society.
Imec is headquartered in Leuven, Belgium, and has offices in Belgium, the Netherlands, Taiwan, US, China and Japan. Its staff of more than 1,750 people includes over 650 industrial residents and guest researchers. In 2008, imec's revenue (P&L) was 270 million euro.
Further information on imec can be found at www.imec.be.

Intel is the world's largest chip maker, and a leading manufacturer of computer, networking and communications products. Intel Barcelona Research Centre (IBRC) is one of the Intel Labs. Its activities focus on research in the areas of microarchitecture and compilers for future microprocessors with the objective of increasing their performance and reducing their energy consumption and cost, while delivering highly reliable systems. IBRC has a long experience in the area of resilient microarchitectures, and has published many papers in this area.

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