Speck Assembly and Packaging

Sensor Networks in ADS Applications

Thursday,

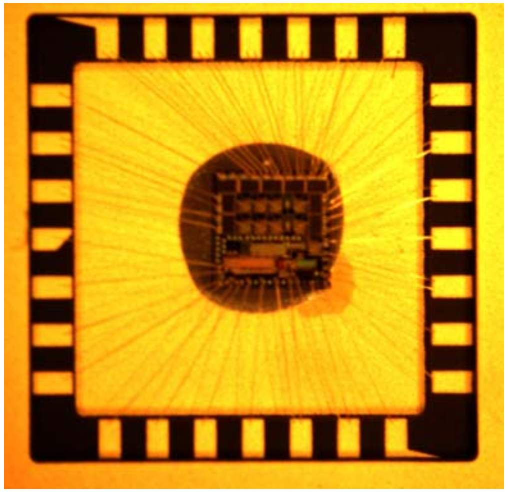
7th September 2006

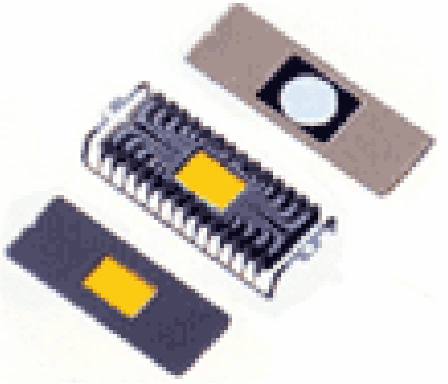
The Purpose of Packaging

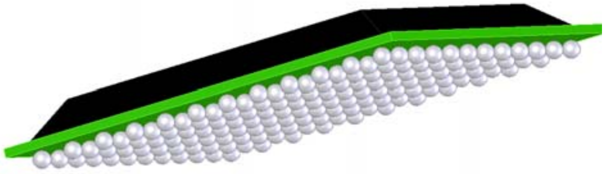
- Environmental Protection
  - Mechanical protection
  - Isolation from moisture, oxygen etc. as required
  - Protection from unwanted electrical (EMC) or optical influences
  - Provides optimised thermal pathway
- Connectivity
  - Allows small device to interface to next level
  - Provides power connection for device operation

Basic Packaging Processes

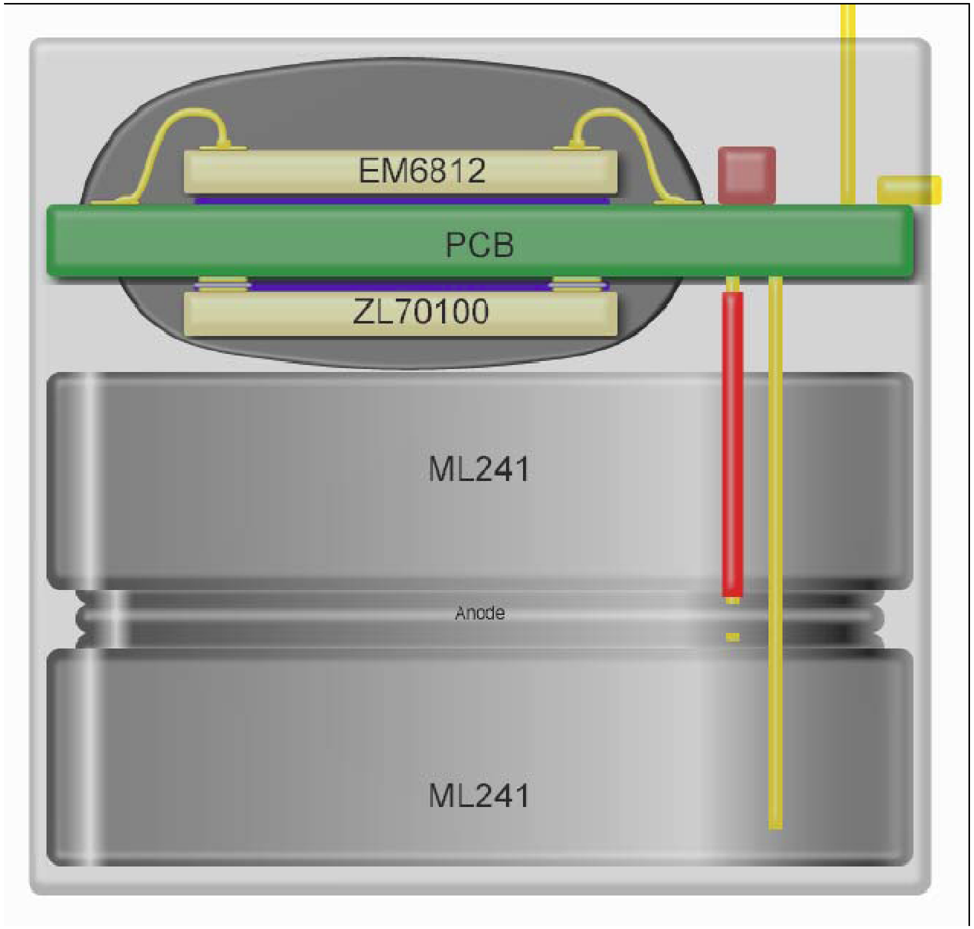
- Wafer dicing
- Die pick
- Die attach
- Wire bond/flip chip attach
- Encapsulate/seal
- Lead finishing
- Trim and form
- Marking





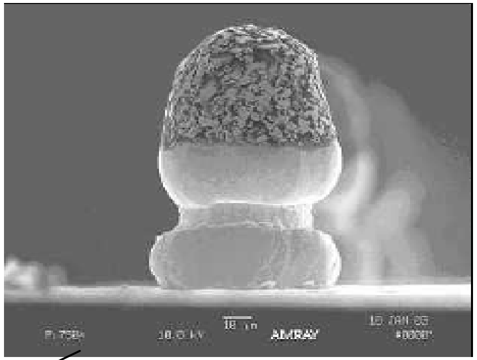


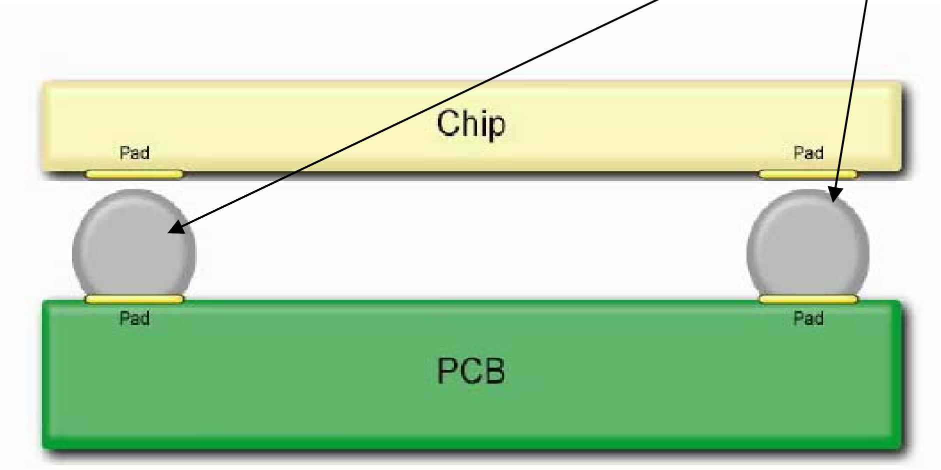
5Cube OTS Assembly



Flip Chip Assembly

- Smallest size
- Highest performance
- Greatest I/O Flexibility
- Most Rugged
- Lowest Cost
- Uses bumps:

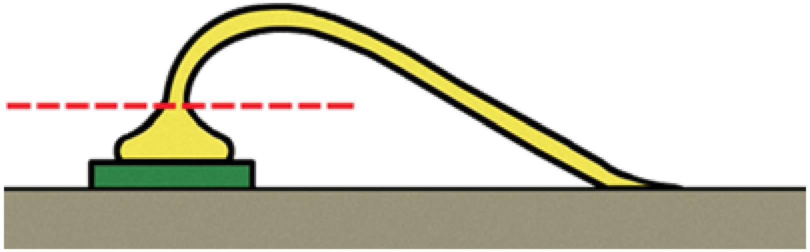




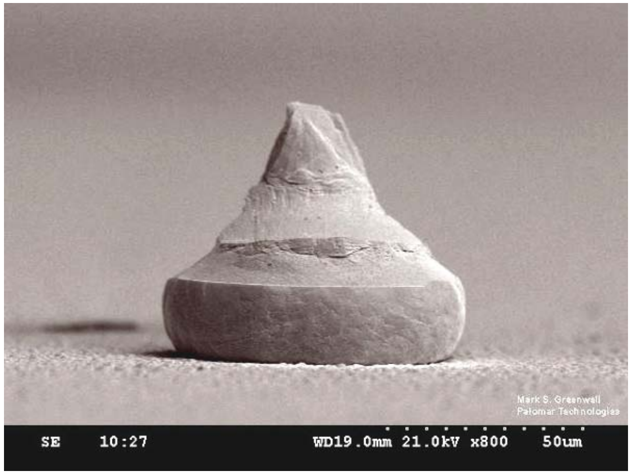
Bumps

- Provide
  - Electrical conductive path
  - Thermal conductive path
  - Mechanical mounting
  - Spacing and mechanical strain relief
- Solder bump
- Plated bump
- Adhesive bump
- Gold Stud bump – can be applied to single die or wafers – unique!
- Under fill
  - protects bumps against moisture and other environmental hazards
  - adds to mechanical strength
  - compensates differential thermal expansion by “locking” chip and substrate together.

Ball Bump from Wire Bond



Ball Bumps are created by forming a tail rather than loop



Coin

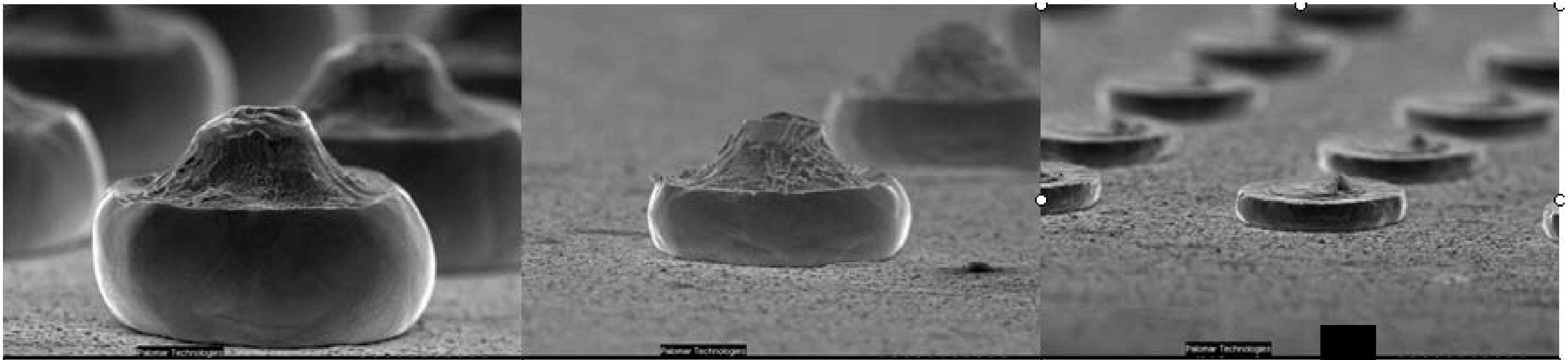
$WIP
$Process
$Yield

Ball Bump before Coin

Ball Bump after Coin

Ball Bumps Shapes and Sizes

planarBump™

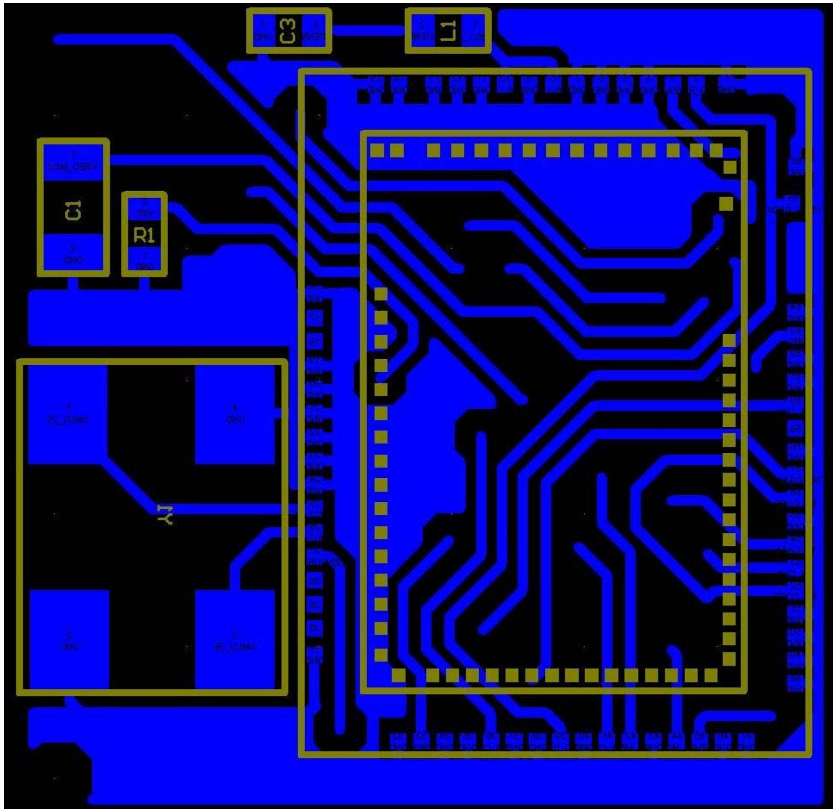


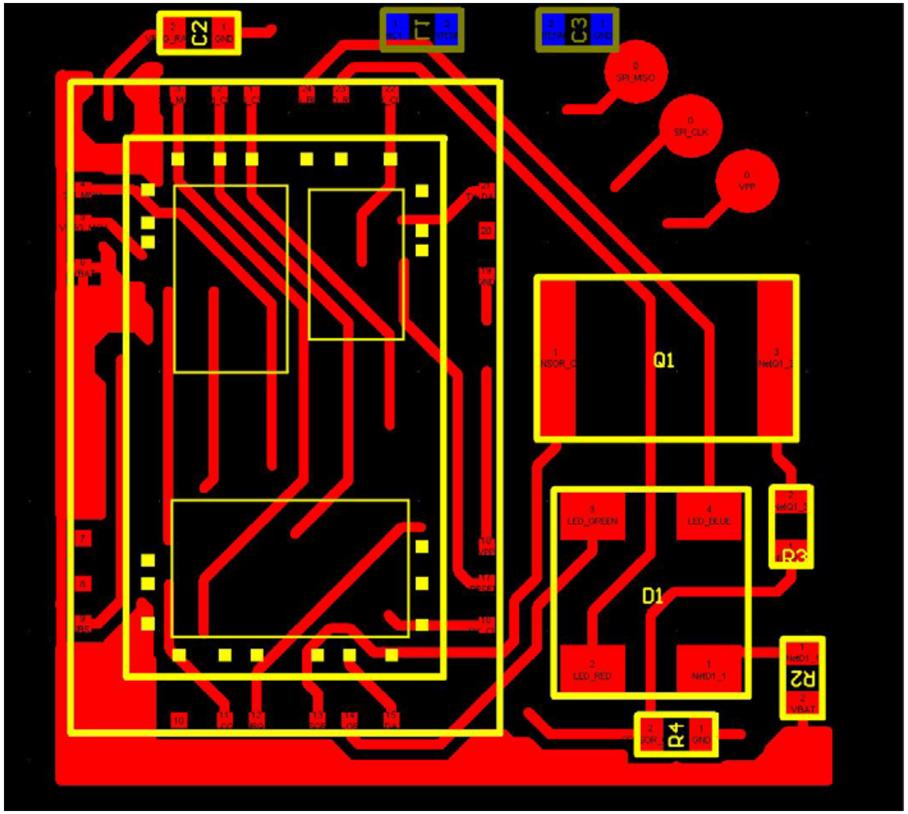
MBD = 130 um TH = 100 um Aspect Ratio = 0.77 A	MBD = 100 um TH = 70 um Aspect Ratio = 0.70 B	MBD = 72 um TH = 20 um Aspect Ratio = 0.28 C

Bump Shapes and Sizes at 600X (Relative Comparison) A) Large ball; B) Medium ball, and C) Small flat top ball no neck (planarBump™).

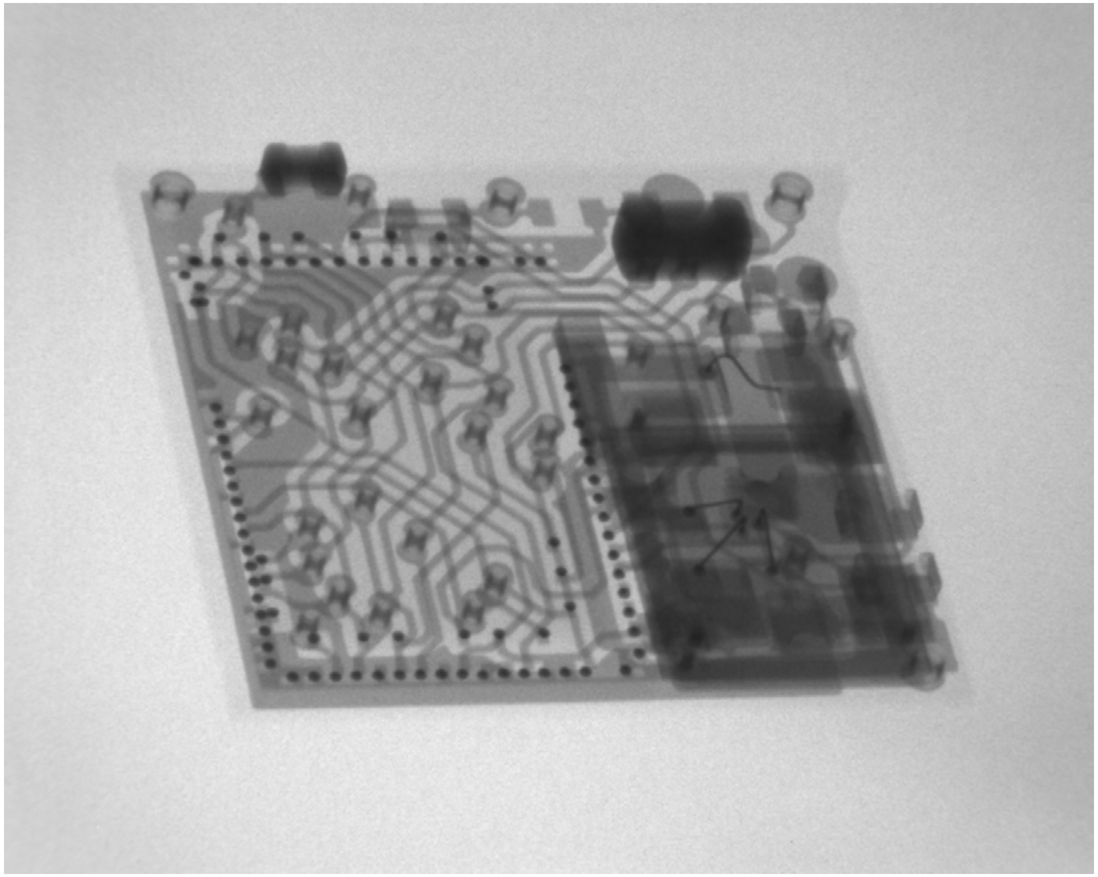
Mashed ball diameter (MBD), Top Height (TH), and Aspect Ratio (TH/MBD)

5CubeOTS PCB Bottom and Top Layout



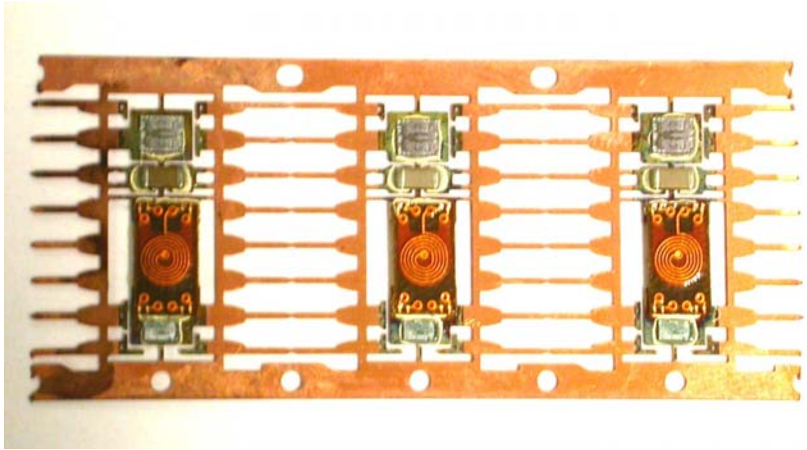


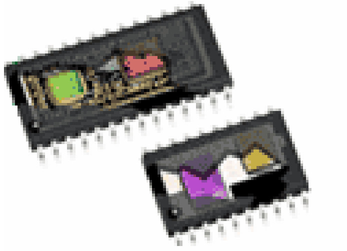
5CubeOTS PCB Assembly (X-Ray)

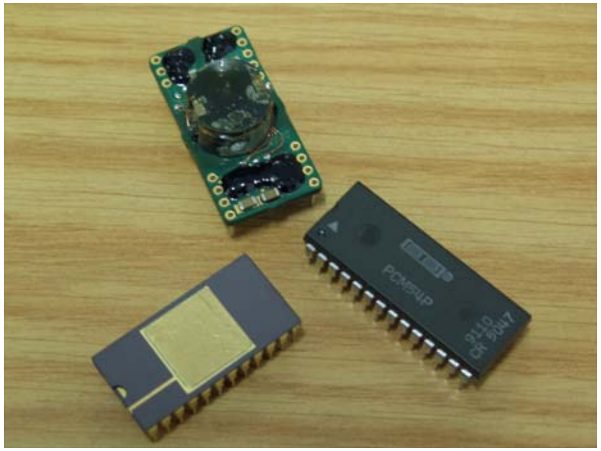


Standard Packages

- Non-hermetic
    - Moulded plastic, leadframe, chip on board, BGA
    - Volume assembly, large installed base
    - Glob-top on substrate (COB)
    - Chip Scale Package (CSP)





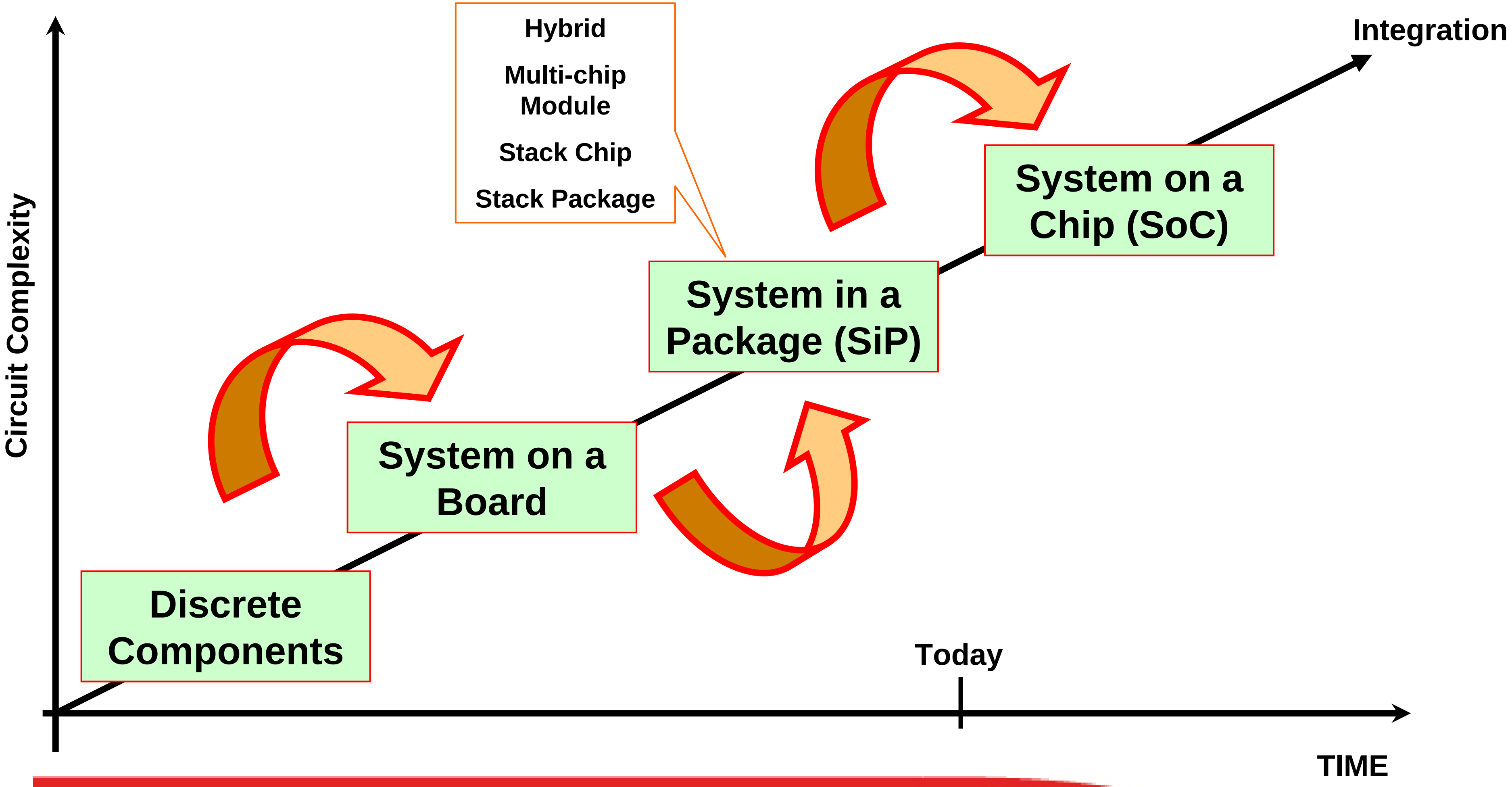


- Hermetic
    - Ceramic and metal packages
    - Many custom types in use
    - Primarily low volume
    - Commonest for opto

Advanced Packaging Requirements

- Trend toward increasing system integration at die/package level
  - Need for smallest form factor
  - Requirement for different devices/passives to be in close proximity e.g. RF applications
  - Development of concept of Multi Chip Module (MCM) and System In Package (SiP)
  - Increasing functionality on silicon die leading to concept of System on Chip (SoC)
- Sophisticated high pin count substrate based packaging being developed

Packaging Integration - Evolution



Hybrid

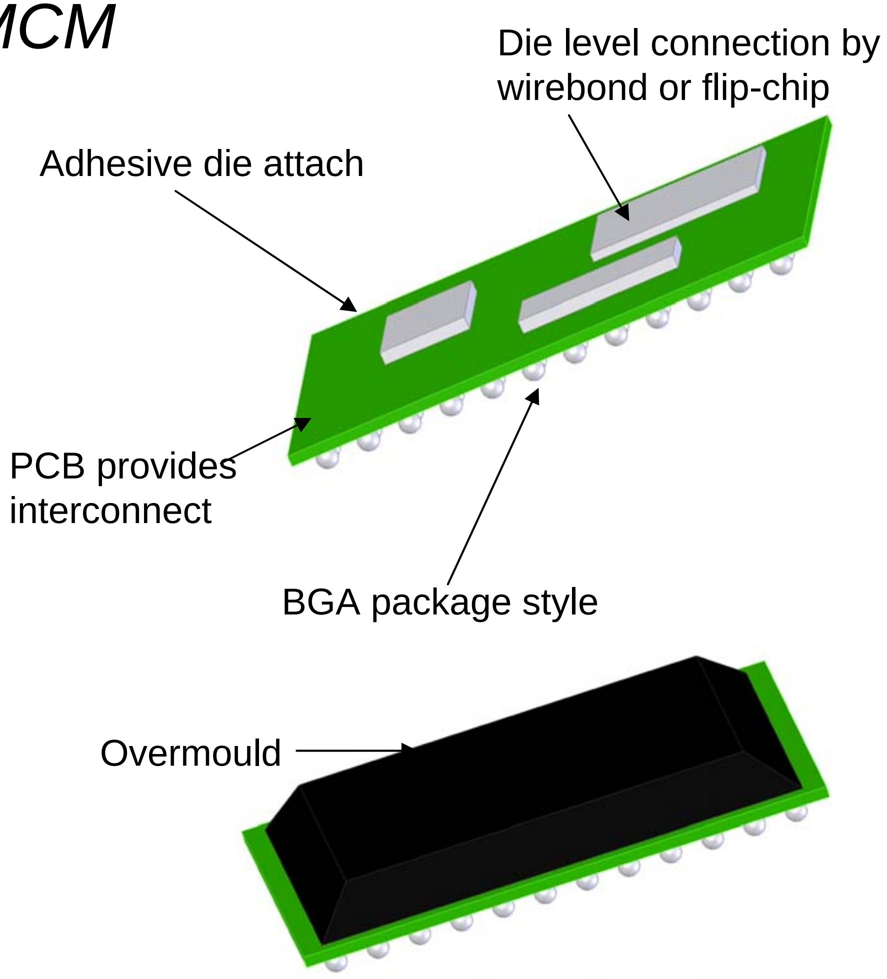
Multi-chip Module

Stack Chip

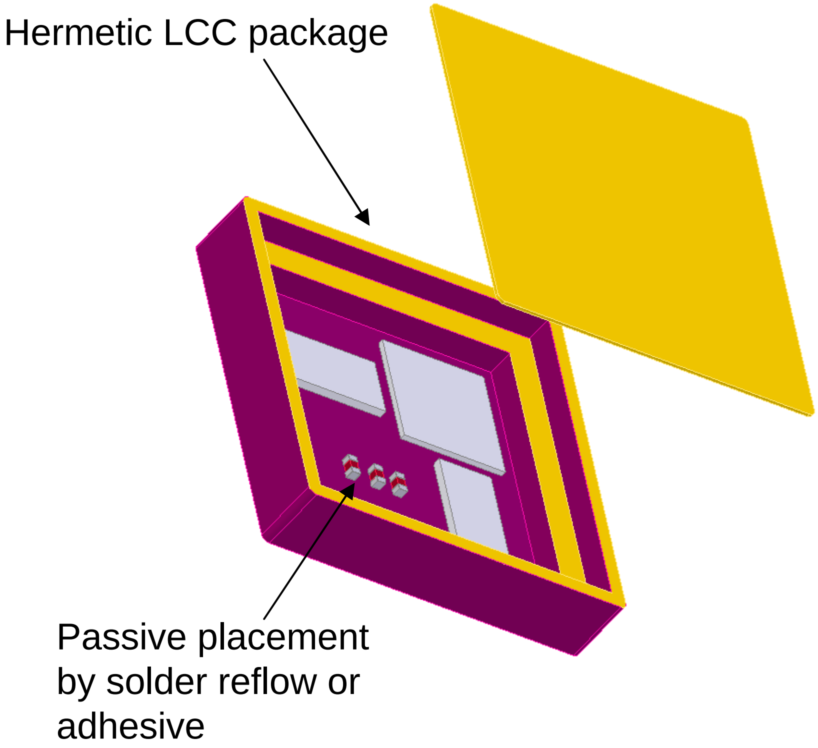
Stack Package

MCM

- MCM is an established technology
- In use at IBM in the ‘70s as a way of providing higher integration with known-good-die
- Commonly die and passives in a single layer on an interconnect substrate
- Many applications in RF and Opto
- Both hermetic and non-hermetic packaging methods



MCM



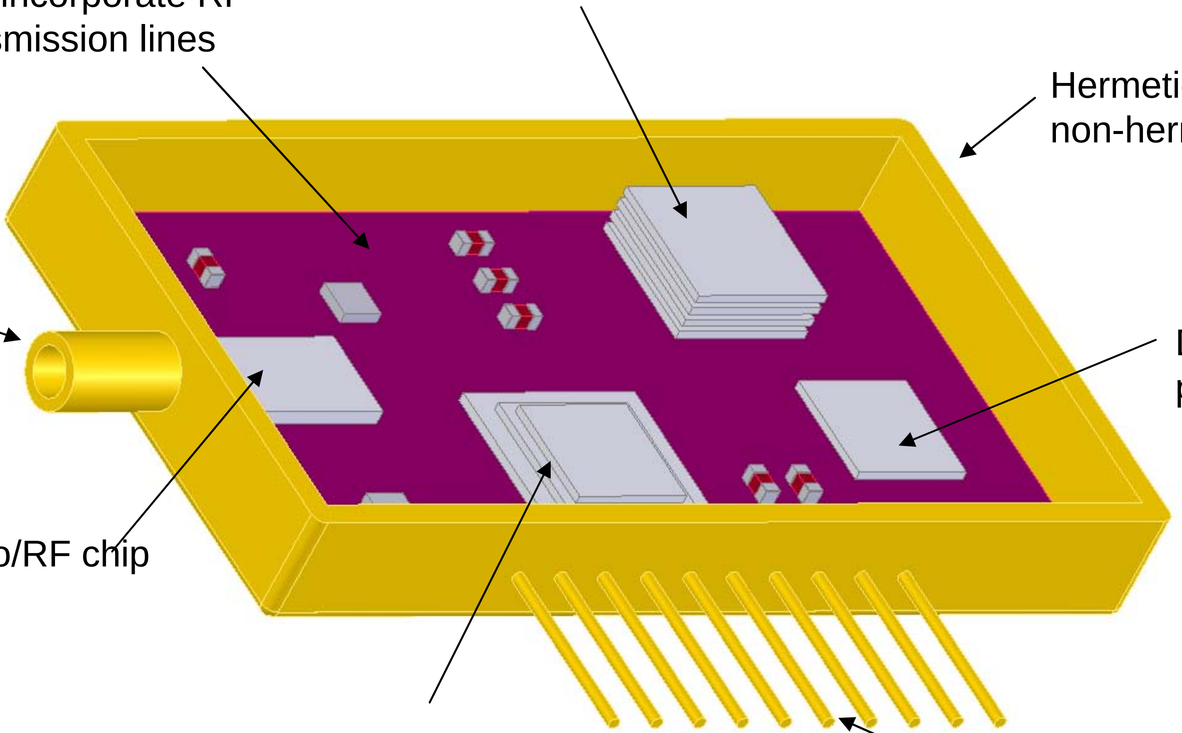
- Increasing substrate/package sophistication
  - Finer track/gap
  - Multilayer
  - Integration of passives
  - Improved RF performance
  - Opto feedthroughs
- Higher integration and packaged module performance

- *Concept of “System in Package”*

System in Package - SiP

- Extension of MCM concept
- Provision of full system functionality in small form factor
- Allows integration of dissimilar chip technologies e.g. CMOS logic on Si with III/V RF components
- Can accommodate optical and MEMS devices with required peripheral components
- Can include vertical interconnection, “die stacking”
- External package is typically custom and may be hermetic

SiP



Multilayer substrate may incorporate RF transmission lines

Bumped die on interposer

Hermetic package
non-hermetic also possible

Optical or RF feedthrough

Discrete die and passives placed

Opto/RF chip

Wirebonded stacked die

Pin interconnect
also surface mount

SiP - Technology

- Enabling technologies for SiP now widely available
- Increasing complexity of consumer electronics, combining different chip technologies and the ongoing requirement to reduce product size and cost a major driver for this technology
- Many large companies, in the electronics sector, are now using or developing SiP based products
  - Intel, Mitsubishi, IBM, Fujitsu, Sharp, Toshiba etc.

Die Level Convergence - System on a Chip

- Increasing integration at die level has opened up the feasibility of having all the electronic functionality for a system on a single silicon chip – System on a Chip (SoC)
  - Smallest possible form factor
  - Economy of scale in manufacture => lowest possible unit cost
- This concept is not recent and has long been sought by major chip manufacturers
- Many successful chip designs combine different functions on a single chip e.g. logic and memory in microprocessors

SoC

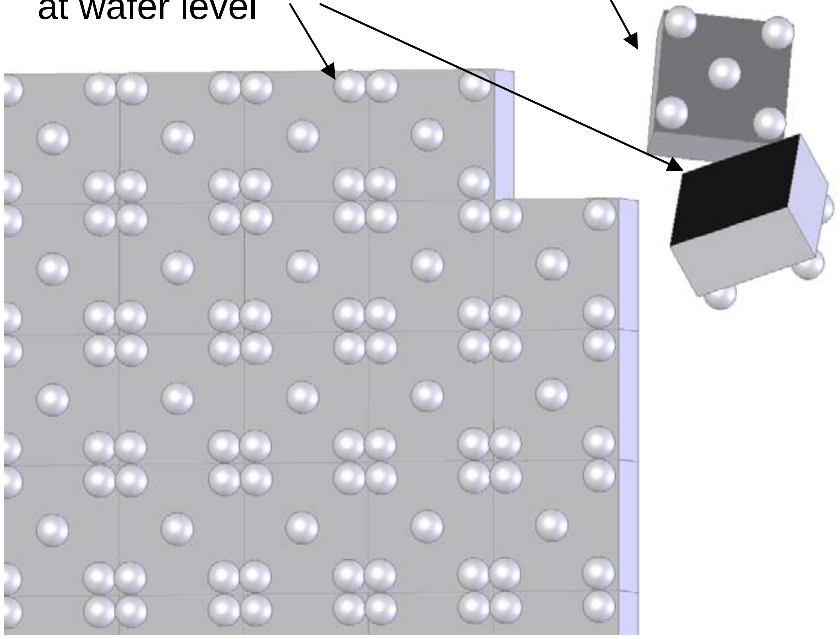
- Not all required electronic functions can be readily manufactured in Si
  - Capacitors
  - Filters
  - Waveguides
  - Optical components
- Different Si wafer fabrication technologies are required for different electronic functions
  - CMOS for logic
  - Bipolar for power components
- Die level design and tooling is expensive

Trend to Further Integration – Wafer Level Packaging

- Ongoing industry need for space saving at board level
  - Mobile phones, PDAs etc.
- Smallest possible size package is die size
  - Chip Scale Package (CSP)
- Need for protection of die surface as soon as possible after fabrication
  - Particularly applicable to MEMS

CSP

- Die designed for CSP
- Small die only
- Economy of scale from wafer level processing and minimal packaging materials
- Die is package
  - Area array pads with bumps
  - Die surface protected by passivation
  - Die backside typically coated with epoxy
  - Die edge is package side



Chip separation by wafer saw

Die bumped and coated at wafer level

Wafer Level Packaging - WLP

- WLP is generally defined as formation of the complete package before die separation as in CSP
- However, encapsulation (capping or coating for die protection) and formation of the die interconnects (bumping) are major steps, commonly viewed as packaging, now often carried out at wafer level for varying device types including large complex semiconductors (microprocessors) and MEMS sensors
- Value add from reduction in contamination/damage risk in further handling and so improved yield

Systems Packaging Tradeoffs

	Cost	Performance	Technology Status
SoC	*Initially expensive to set up – high design, tooling and prototyping costs. Though uses established processes.* *Production unit cost is lowest for high volume.*	*For CMOS integration the best performance.* *Difficult to integrate most other electronic and sensing functions.*	*Well established but few implementations across different technologies and ultimately limited.* *The best for suitable applications*
SiP	*Moderate costs to initiate, still requires substantial NRE and design. Uses established processes. Low unit cost in medium to high volume.*	*Particularly suited to RF and opto applications. Latest processing techniques can ensure excellent performance.*	*Well established and rapidly developing in terms of packaging materials and techniques.*
WLP	*Initially expensive to set up. Using many developing processes. Unit cost of finished part likely to be very low at high volume.*	*WLP is an enabling technology to improve chip yield and package size/cost reduction. The techniques show good performance in achieving this.*	*CSP is well established. Encapsulation of more complex parts at wafer level is costly and typically proprietary.*

Systems Packaging Tradeoffs – Conclusion 1

- Package Type
  - Ceramic/metal can
    - Full hermeticity, compatible with RF/opto, many i/o possible. Due to technology very fine pitch not possible so package footprint is larger and not compatible with high volume surface mount. Typically the most expensive package style and usually at least part custom so attracts NRE but with high performance and reliability has many applications for complex SoC and SiP.
  - Plastic moulded/Chip on Board
    - Non-hermetic, commonest volume packages but suited only to limited RF/opto applications. Moulded on leadframe and overmoulded PCB parts can have many i/o, at fine pitch and are surface mount compatible. Glob topped COB is very low cost. Many standard configurations so typically low NRE. Reliability can be very good when matched to application. Widely used for SoC and SiP.
  - Chip Scale Package
    - Non-hermetic. Best for small pin count CMOS technology die so potentially well suited to smaller SoC. Lowest unit cost and proven reliability in suitable applications.

System Packaging Tradeoffs – Conclusion 2

- System Complexity
  - With complexity
    - Interconnect (wirebond, solder joint) count increases
    - Number of die/component placements increases
    - Number of process steps increases
  - Increases risk of yield loss and gives poorer reliability
- SiP reduces this risk
  - Fewer joins
  - Combining processes
- SoC reduces it further
  - Minimum interconnects
  - Reliable wafer processing

System Packaging - Conclusions

	Conclusions
SoC	•Can significantly reduce unit costs at fabrication and packaging •NRE can be high •Ultimately limited by wafer fabrication technology •Best for CMOS technology integration
SIP	•Significant cost saving on discrete components •Board area saving and performance improvements •Technology improving, not limited yet •Best solution for mixed technology
WLP	•Lowest cost/smallest size components •NRE can be high •Primarily an enabling technology for packaging •Good for small area die (CSP) or to provide best protection for sensitive parts (sealed MEMS)

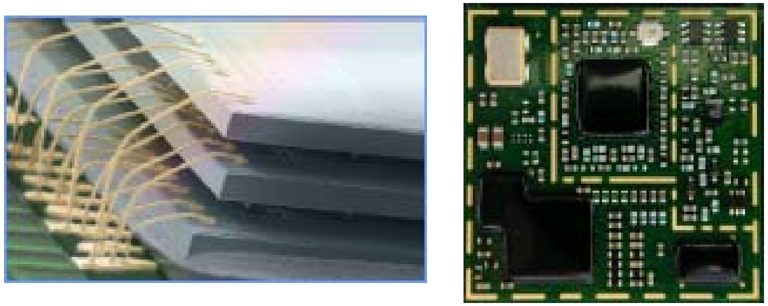
SiP and SoC

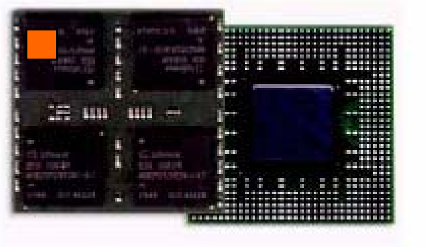
SIP

- Flexibility
- Shorter Development Times
- Performance enhanced
- Mixed Technologies
- Cost reduction over discrete

SoC

- High Performance, control and repeatability
- Further saving in board space
- Lowest device cost
- Reduce packaging costs





- SiP and SoC are not mutually exclusive concepts
  - Most SiP products contain SoC
  - Where technically and economically feasible use SoC

Packaging – Generic Cost Comparison

- Standard Packaging Costs: Volume
  - Plastic leadframe, single die “cent per lead” for whole package.
  - COB on single/dual layer board cheaper still at low pinout.
  - Ceramic/Metal can, low pinout, unit price for package a few dollars.
- Die attach cost greatly reduced by “matrix” approach with many sequential attaches. Favours non-hermetic.
- Typical wirebond cost ~1 cent. Integration saving can be significant for low pinout module.
- Ideal is CSP: package cost is reduced by wafer processing of many units simultaneously with no additional interconnect (die attach, wirebond) cost.

Packaging – Generic Cost, a simple metric

- For a simple system, consisting of a few ICs, a sensing element and a few passives, relative unit cost may be:
  - Separately packaged discretes 100%
  - SiP, PCB substrate with glob top, best integration ~60%
  - SoC, system placed in single plastic package ~40%
  - SoC, system of single die presented as CSP ~30%
    - A significant part of this saving comes from the final board area saving realised by the smaller package footprint
- This comparison does not take into account NRE
- Assumes custom designed ICs and very low i/o count.

Conclusions - Overall

- Systems can be integrated into a single package
  - It is important to match up the system technology and performance to the packaging method implemented
- Packaging integration is a route to
  - Better system performance
  - Higher unit yield
  - Easier volume processing
- And therefore
  - Lower cost