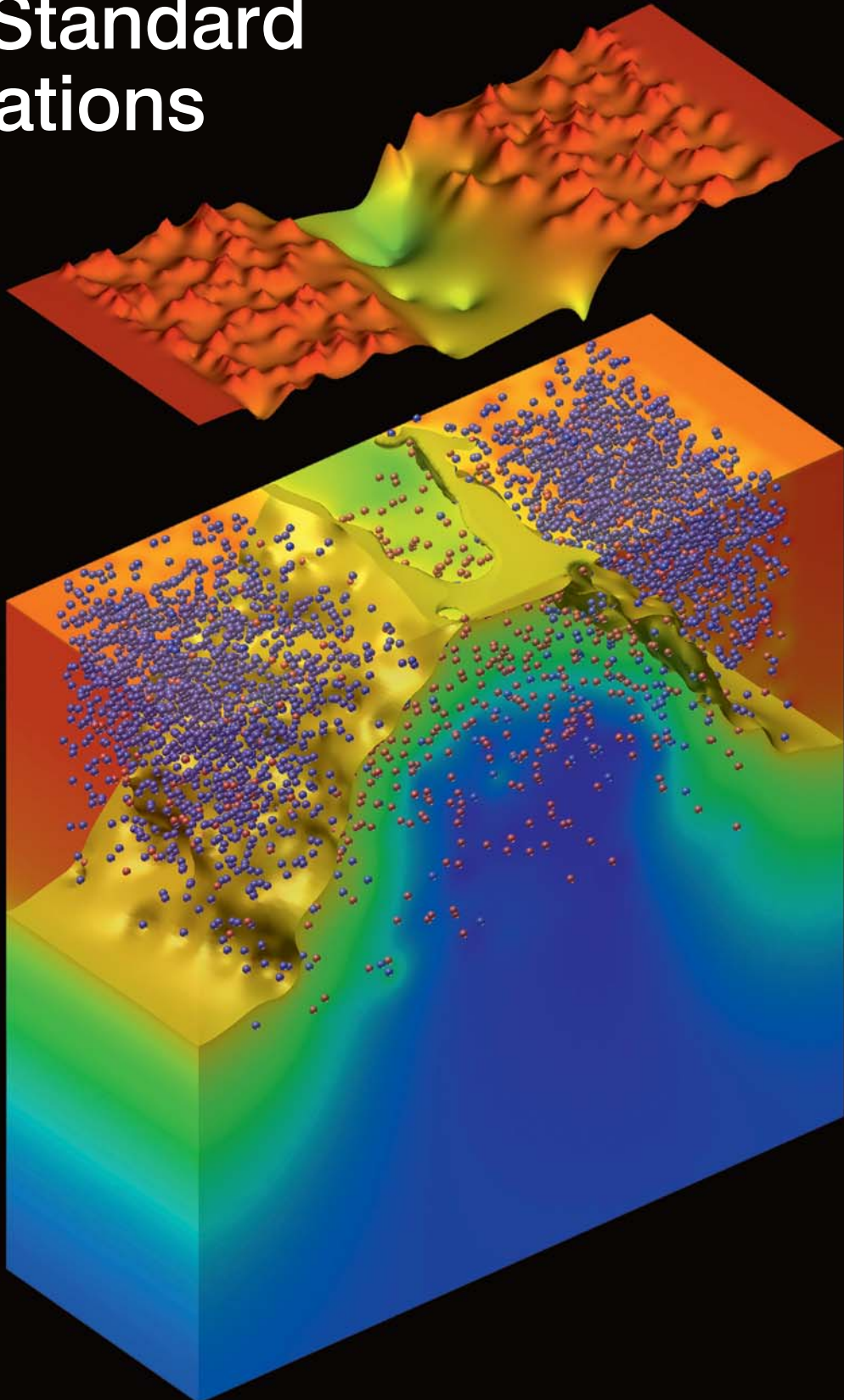




University
of Glasgow

Gold Standard Simulations



Gold Standard Simulations

A spin-out company from the University of Glasgow is developing world-leading technology that could save the semiconductor industry billions of pounds from silicon chip failure by predicting how performance will be affected in future generations of miniature transistors.

Intel founder Gordon Moore correctly predicted in the mid-1960's that increasing miniaturisation would make it possible to double the number of transistors on a microchip every two years, leading to a phenomenal increase in computing power.

A typical silicon chip contains one billion transistors – electrical switches at the heart of microchip complementary metal oxide semiconductor (CMOS) circuits - that have led to an explosion in the capability of devices such as iPods, mobile phones, computers and games.

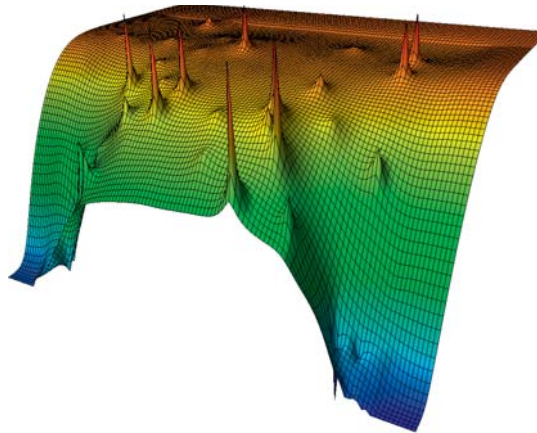
However, as transistors have gotten ever smaller, their performance at nanoscale has started to vary due to atomic imperfections in their structure – a phenomenon known as 'statistical variability'. This has led to decreasing yield and increasing rates of chip failure for the \$300 billion a year semiconductor industry. It can take companies on average 18 months to bring a new product to market and delays caused by chip failure can lead to businesses losing millions of dollars of market share.

Gold Standard Simulations, a new spin-out company headed by Professor Asen Asenov at the University of Glasgow's School of Engineering, is leading the world in predicting 'statistical variability' in microchip performance.

His Device Modelling Group at the university has developed the most sophisticated and accurate three dimensional tools in the world for simulation and prediction of the statistical variability in nano-transistors.

Gold Standard Simulations uses these tools to predict variations in the performance of next generation transistors two years before they come to market, allowing the semiconductor manufacturers who design them to modify them to improve performance and yield.

Prof Asenov believes these techniques could save the semiconductor industry up to \$2 billion a year now, rising to \$4 billion in



Spikes in the electrostatic potential due to discrete dopan.

the next five years, and Gold Standard Simulations is aiming to be the first to market with these tools.

Gold Standard Simulations was formed this year and its research and development has been facilitated by the Engineering and Physical Sciences Research Council (EPSRC) and Scottish Enterprise funding. Professor Asenov's research group developed the tools in recent years with funding from EPSRC, the European Commission, and the European Nanoelectronics Initiative Advisory Council (ENIAC).

Prof Asenov started the development of the simulation tools 15 years ago when he was approached by NASA, who believed there might be a problem with the randomness of dopants – that are introduced to silicon to make the transistors.

The problem arises because it is impossible to predict how the atomic dopants' atoms will be arranged within the transistors. In what has become known as the Christmas pudding effect, the dopants are like raisins in the pudding mix and no one knows how they will end up positioned in each pudding which exemplifies transistors in the silicon chip. This leads to variations in the current flow and disruptions.

"When we told companies about this 10 years back, they said the transistors are so big we can't see the dopants affecting their performance," said Prof Asenov. "They said it might happen in 15 or 20 years but we can't worry about it now."

"We were lucky to start to develop the tools well before this was recognised by industry. Now the industry has woken up to the fact that this is a big problem and we are the only group in the world that can do the predictive simulation that can help solve these problems."

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